



H61H2-M12

Rev : 1.0

ECS CONFIDENTIAL

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24	AUDIO VT1705/ALC662(CHIP)
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NOTE:
Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev_0_8.pdf,
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip

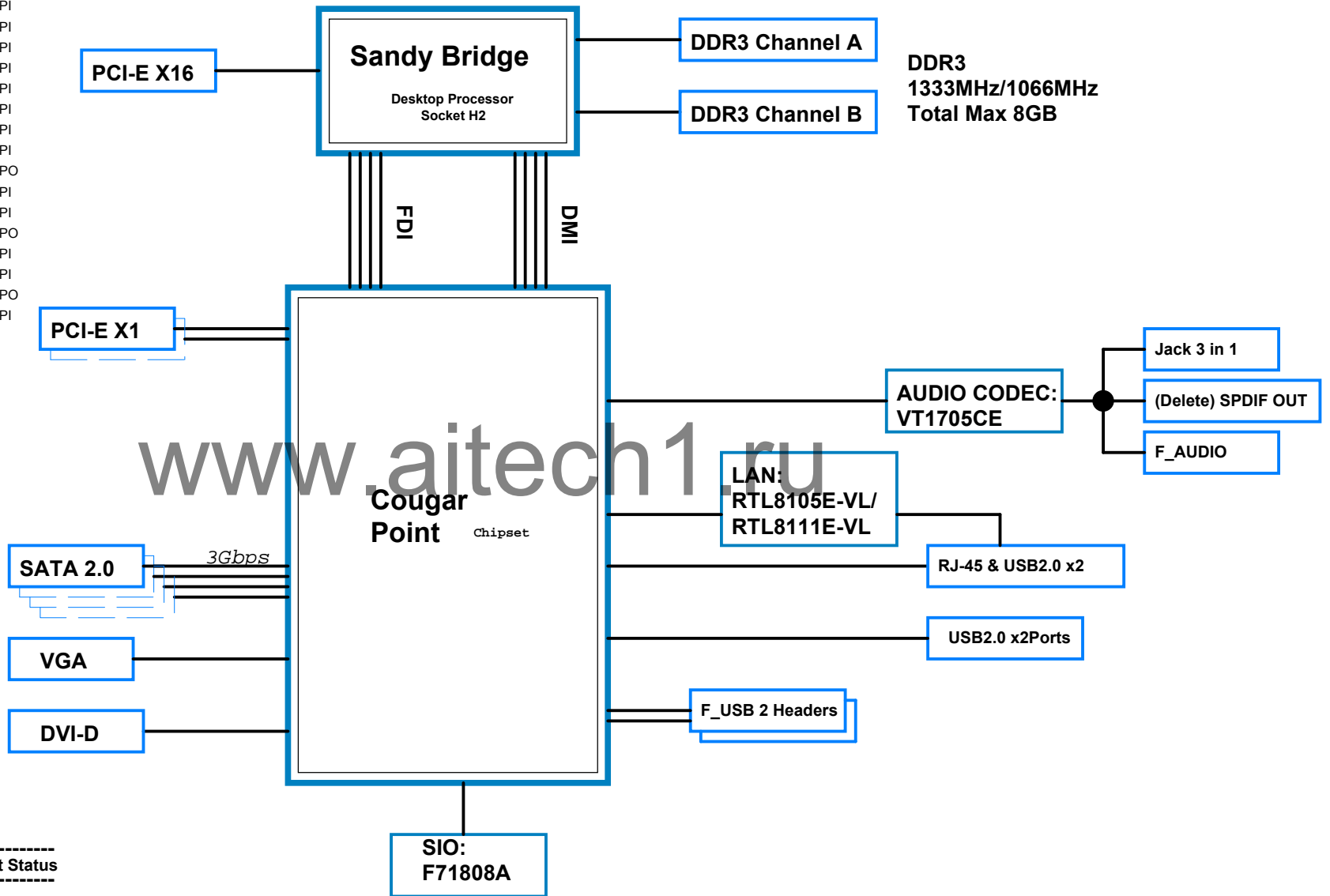
REVISION HISTORY:

Rev	Date	Notes
P61G V1.0	2011/04/07	RED_PCB P/N : 15-Y97-011001 (GE1) / 15-Y97-011000 (CHUANYI) BOM P/N : 81-605-Y97100 EC35 change to EC-cap 1000U-6.3DL EC1, EC4 from 100uF change to 220uF Del RT1, RT3, R137, R180 (Not need compensation of temperature). For 5VSB Inrush Current : R102 from 100k change to 33k. Select TACH0_GPIO17 to decide COM .
H61H2-M12 VA	2011/05/04	Black_PCB P/N : 15-EC7-010010 BOM P/N : 81-605-EC7000/81-605-EC7001(10/100 ; GiGA) PCB Size change to 225*170 mm Del DMI Vcore 減少一相 VIN 電容減少一顆 LAN change to Atheros 8152/8151/8161 Codec change to VT1705CE. USB Power use fuse & Jumper.
H61H2-M12 V1.0	2011/07/12	Black_PCB P/N : 15-EC7-011000/15-EC7-011001 BOM P/N : PCB Size change to 225*170 mm

RD : Jayson
LAYOUT :
EMI :

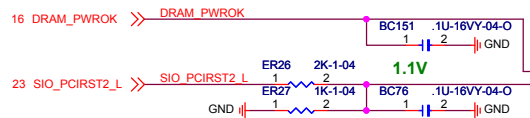
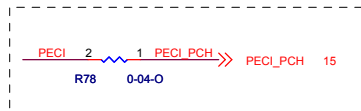
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI
GPIO15	3VSB	Down Voltage for DIMM	GPO
GPIO48	VCC3	Down Voltage for DIMM	GPI



SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
PIN23	5VSB	Power LED	GPIO25/LEDVCC/WDTRST#
PIN22	5VSB	Power LED	GPIO24/LEDVSB
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	



CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFSEL[0]
6	*	*	PEOFSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

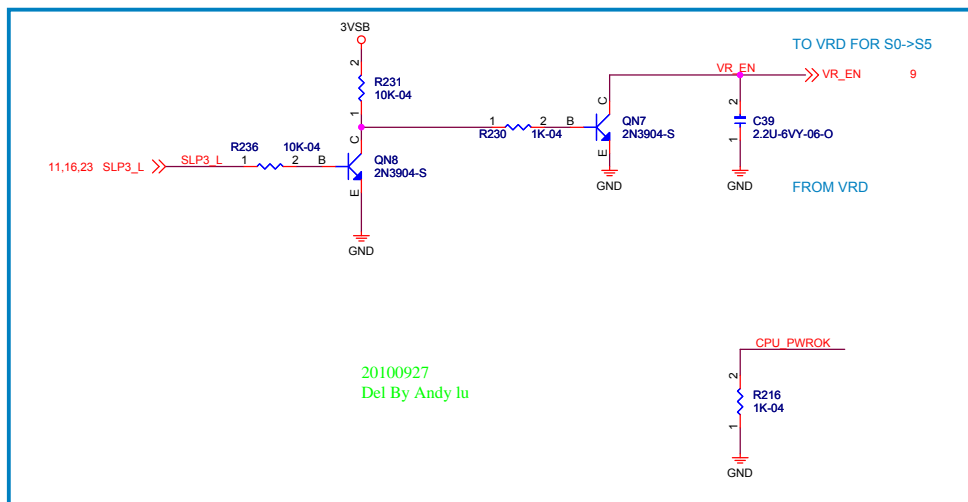
CFG[5:6]:
 01=DEFAULT X16,
 10=RESERVED,
 00=X8,X4,X4

change test point for internal PU Jack05/25

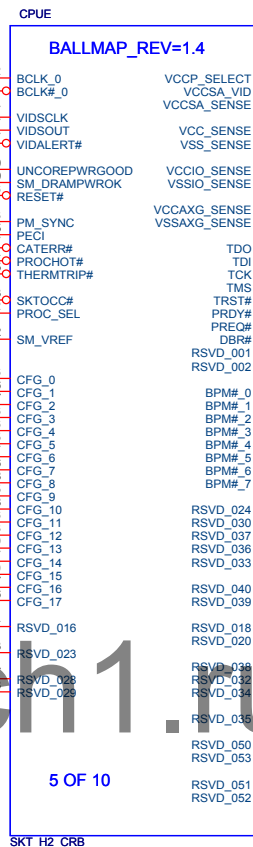
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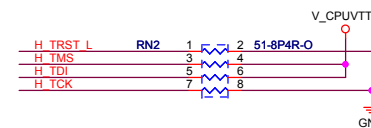
Power Down Sequencing Circuit



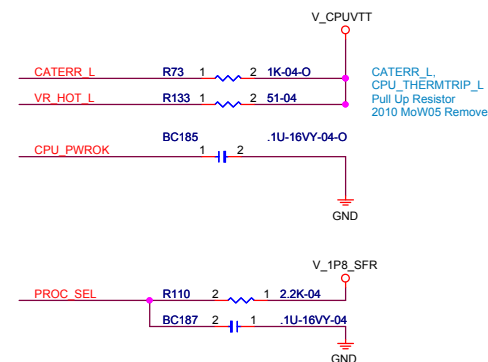
20100927
 Del By Andy lu



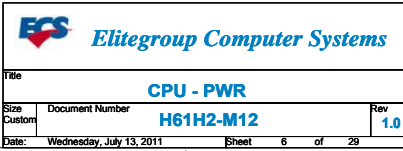
1130*10
 pull high By Jayson Del,
 Pull high on Page11

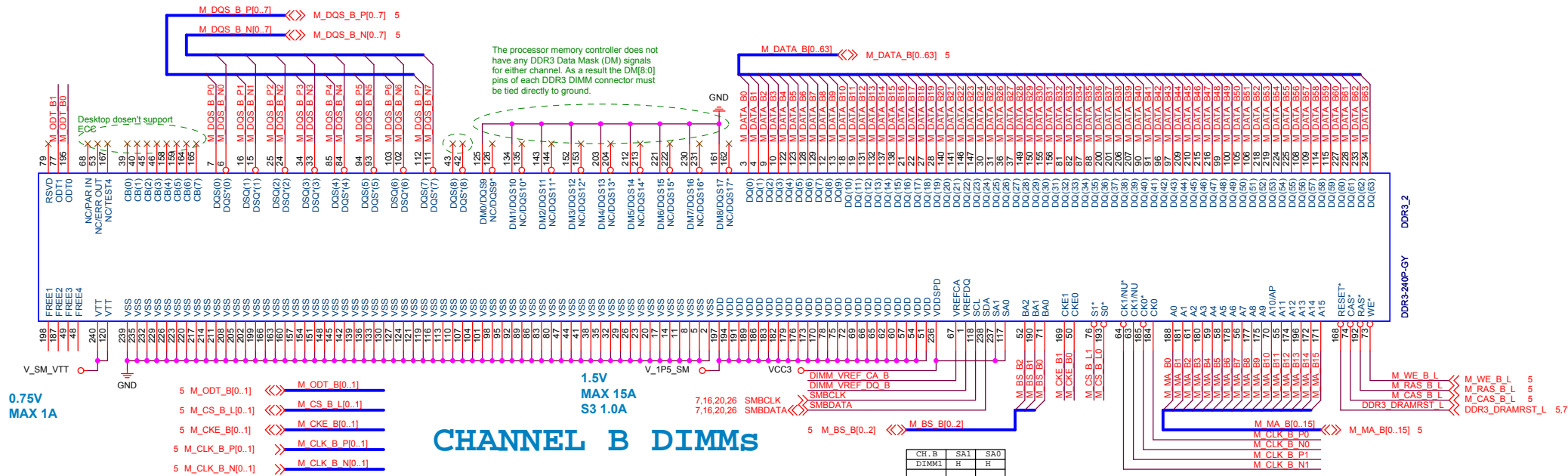


EDS P68/132 has internal PU Jack05/25

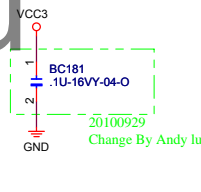
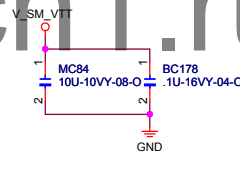
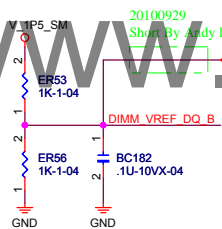
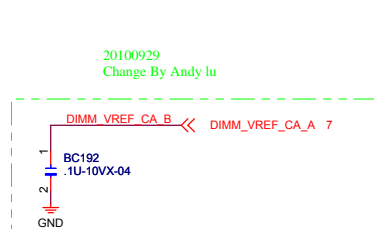


DMI/FDI termination voltage:
 DC coupled: TX/RX to VCC ISF sampled high
 DC coupled: TX/RX to VSS IF sampled low
 AC COUPLED: TX set to VCC/2, RX set to VSS regardless of this strap





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Del DIMM3 for always populate DIMM4 first Jack 05/13

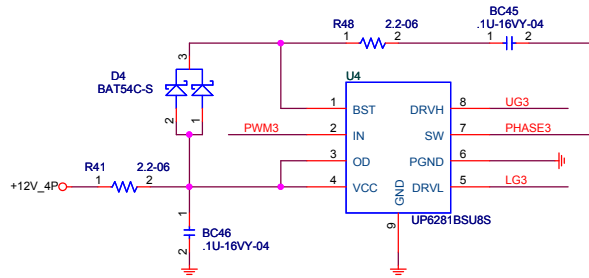
External Connection

VCC
VCORE
VAXG
+12V_4P
VCC3
VIN

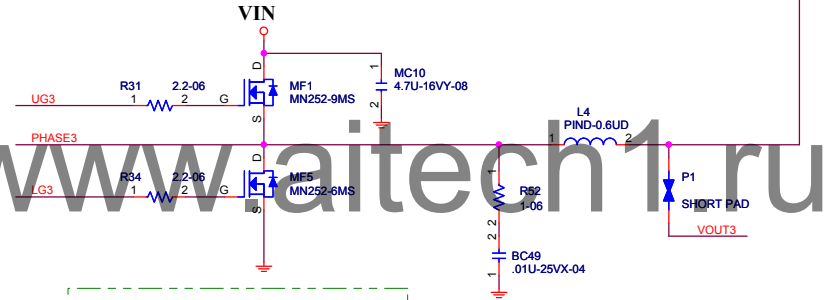
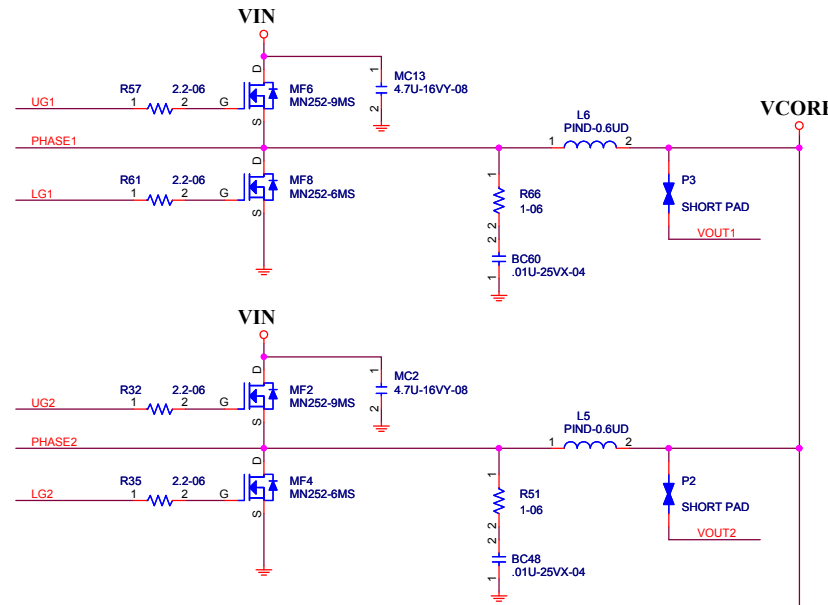
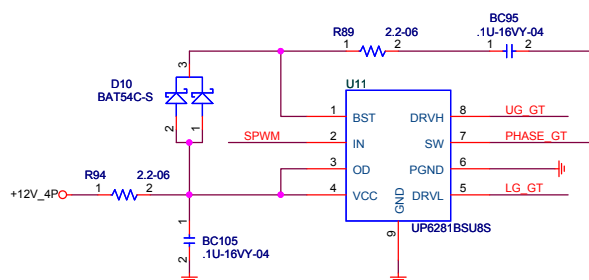
9 UG1
9 LG1
9 UG2
9 LG2
9 PWM3
9 SPWM

9 PHASE1
9 PHASE2
9 PHASE3
9 PHASE_GT

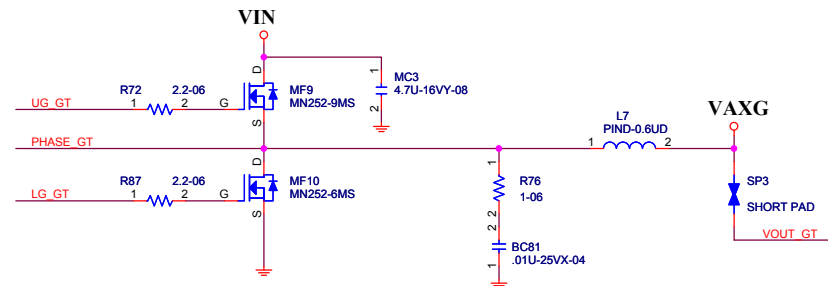
9 VOUT1
9 VOUT2
9 VOUT3
9 VOUT_GT



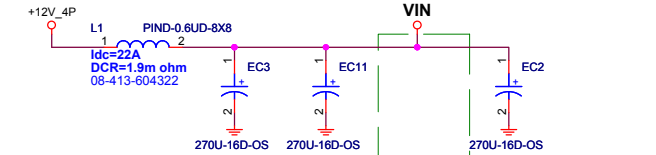
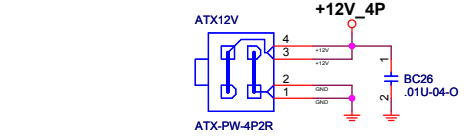
0504'11 Jayson :
DEL Driver



0504'11 Jayson :
DEL Phase 4

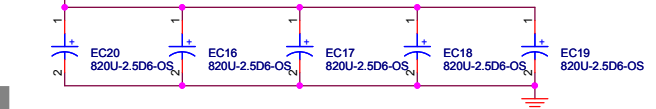


VCORE

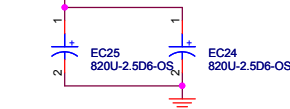


0504'11 Jayson :
VIN Cap Reduce EC10

VCORE



VAXG



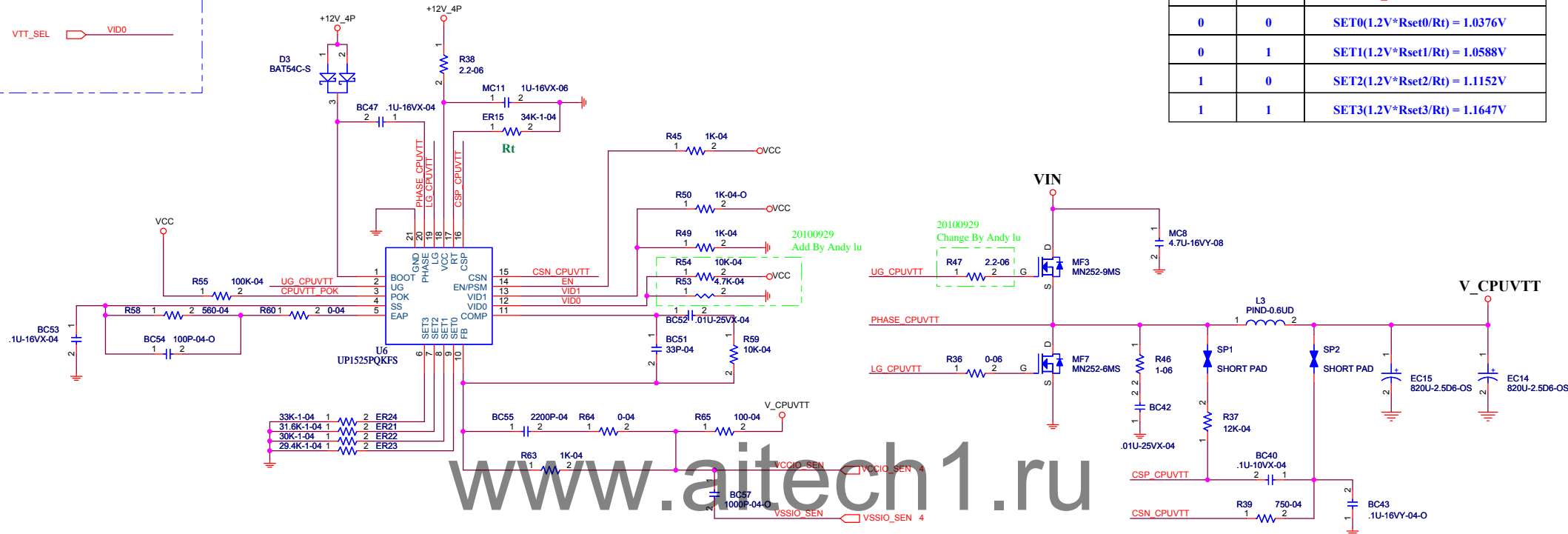
Elitegroup Computer Systems

Title		DC/DC VCORE/VAXG UP6281	
Size	Document Number	H61H2-M12	
Custom		Rev 1.0	
Date:	Wednesday, July 13, 2011	Sheet	10 of 29

External Connection

VCC
VCC3
V_CPUVTT
+12V_4P
VIN

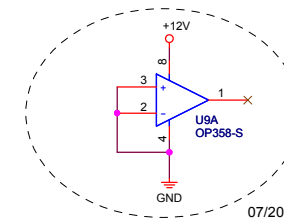
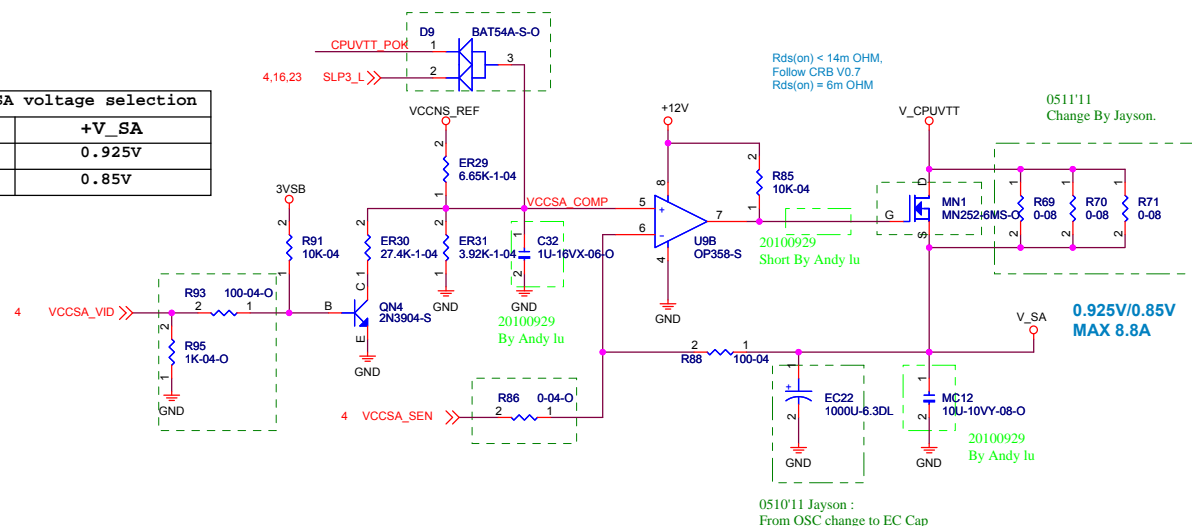
4 VTT_SEL VID0



VID Reference Voltage Selection Table

VID1	VID0	V_CPUVTT
0	0	SET0(1.2V*Rset0/Rt) = 1.0376V
0	1	SET1(1.2V*Rset1/Rt) = 1.0588V
1	0	SET2(1.2V*Rset2/Rt) = 1.1152V
1	1	SET3(1.2V*Rset3/Rt) = 1.1647V

VID	+V_SA
0	0.925V
1	0.85V

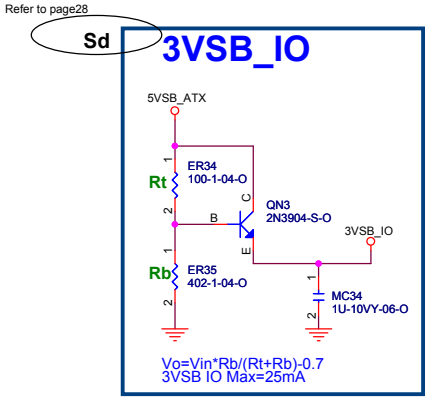
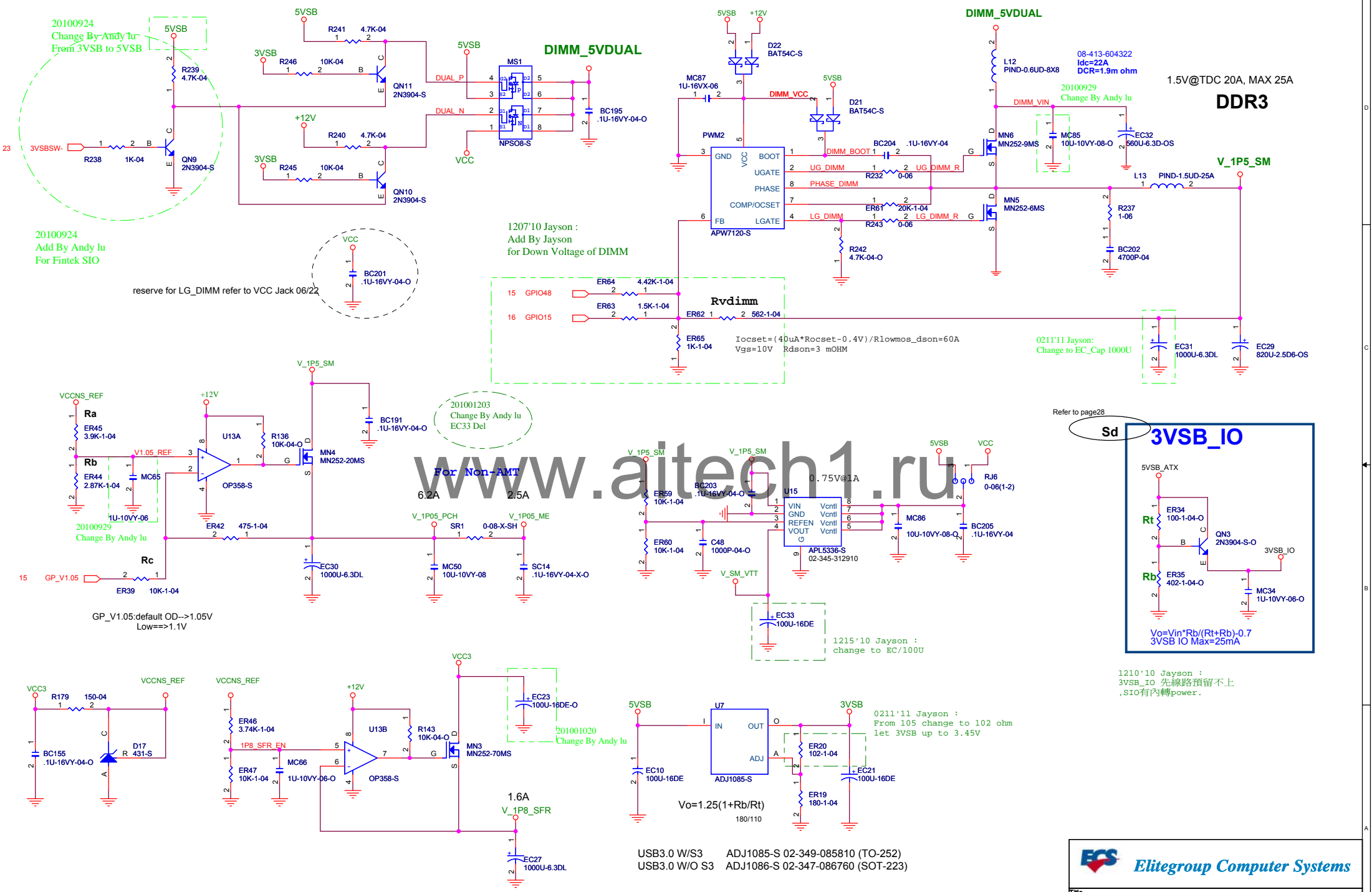


0525'11 Jayson:
D13,R110,R114,R97,MN1先拿掉
R276,R277,R278 上件 +



Elitegroup Computer Systems

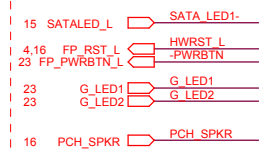
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Size	Document Number
Custom	H61H2-M12
Date	Wednesday, July 13, 2011
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Rev	1.0



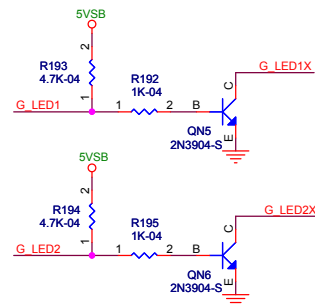
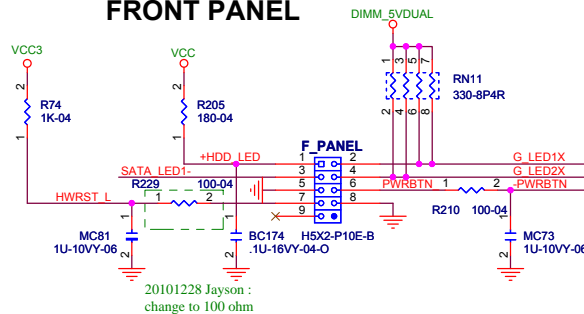
1210'10 Jayson :
3VSB_IO 先線路預留不上
;SIO有內轉power.

USB3.0 W/S3 ADJ1085-S 02-349-085810 (TO-252)
USB3.0 W/O S3 ADJ1086-S 02-347-086760 (SOT-223)

External Connection

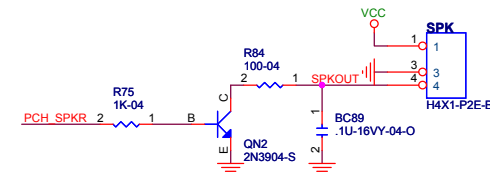


FRONT PANEL



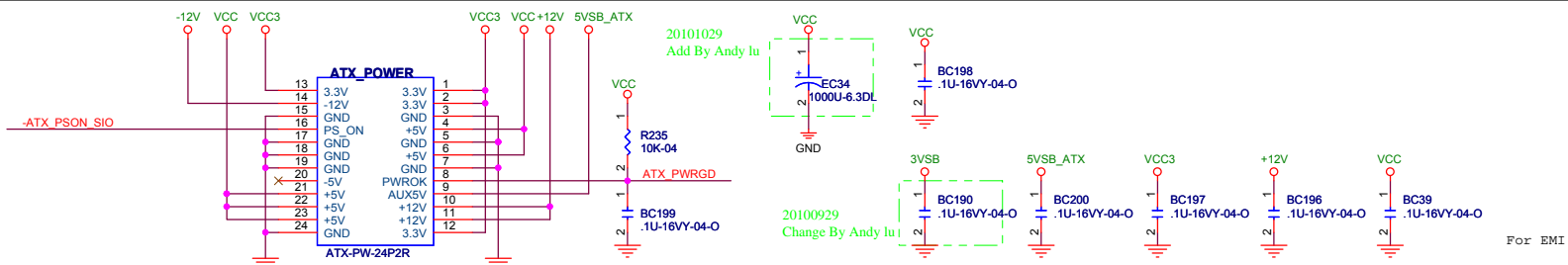
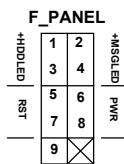
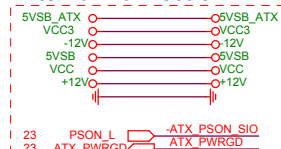
S0	S1	S3	S4	S5
G_LED1	L	B	B	L
G_LED2	H	H	L	L
G	GB	YB	OFF	OFF

B:Blinking



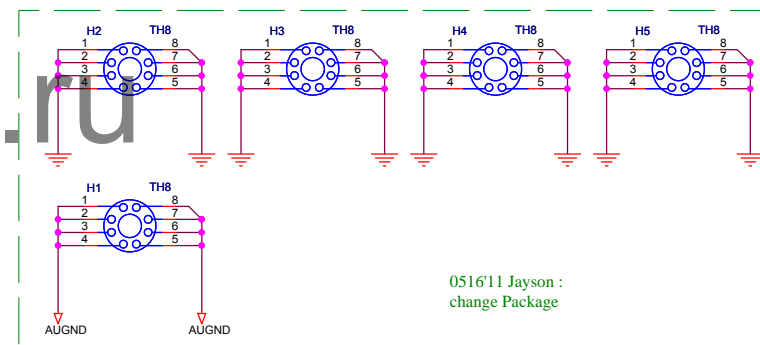
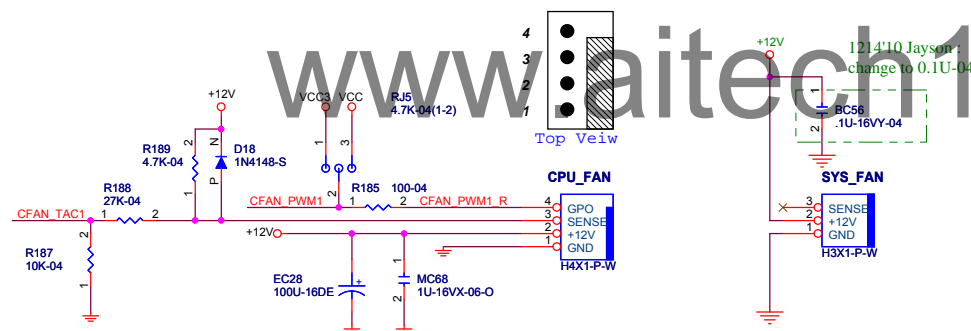
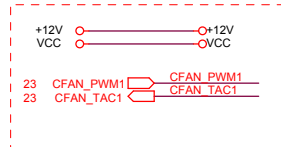
POWER CONNECTOR

External Connection

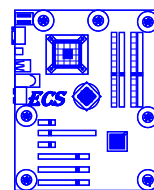


FAN

External Connection

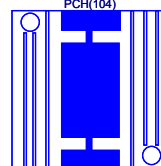


PCB



PCB STACK:

L1:TOP
L2:PWR
L3:GND
L4:BOTTOM



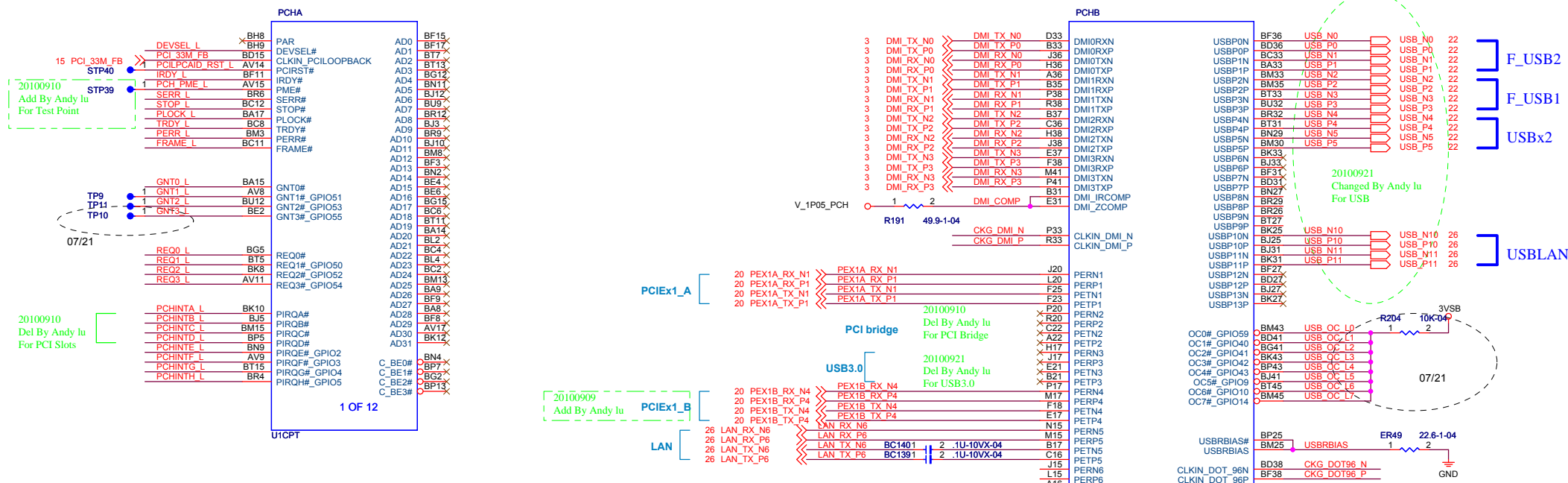
20-120-012242
5series PN:20-120-010851

0214'11 Jayson :
PCH Heat Sink change to smaller.



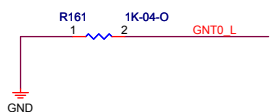
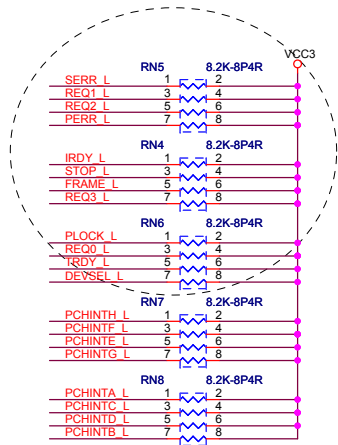
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Front Panel,FAN,PowerConn,GND,104		
Size	Document Number	Rev
Custom	H61H2-M12	1.0
Date:	Wednesday, July 13, 2011	Sheet 13 of 29

For H61:USB Port 6/7/12/13 is disabled....From 440377 file



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For H61:PCIe 7/8 is disable...From intel Jasmine



GPIO19:
Boot Device Select Strap.

GNT0_L:
No More Information in EDS V0.7

GNT1_L:
Boot Device Select Strap.

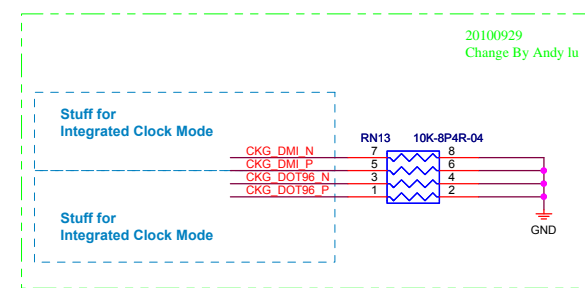
GNT2_L:
ESI Strap (Server Only),
DONT Pull Low in Desktop.

GNT3_L:
Top-Block Swap Override Mode,
When Sampled Low.

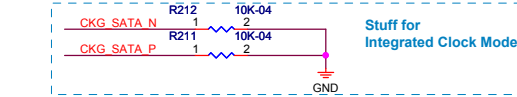
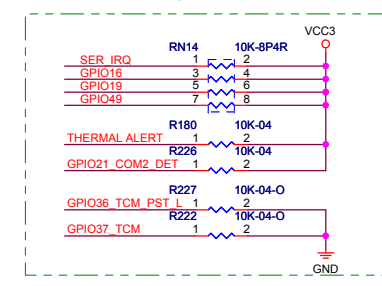
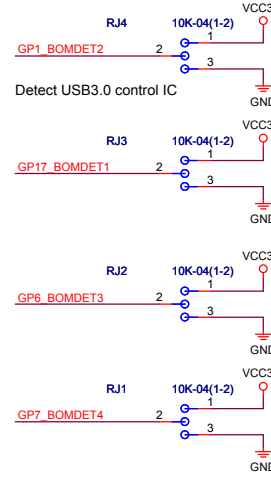
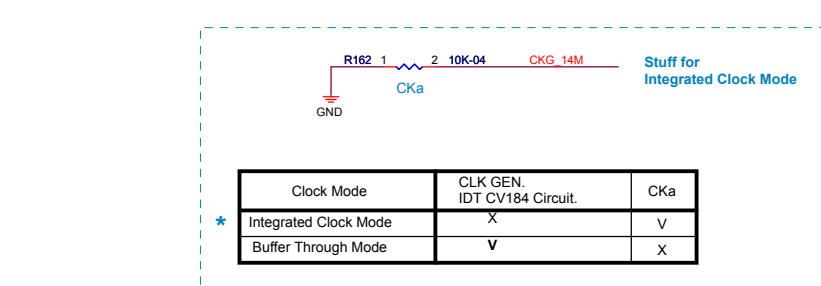
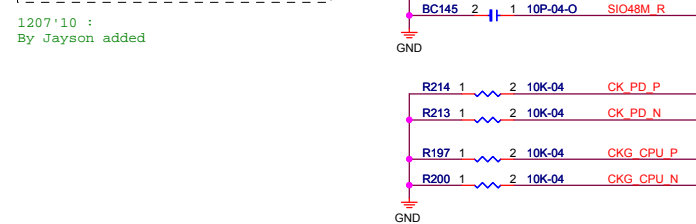
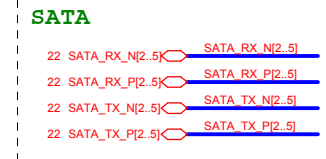
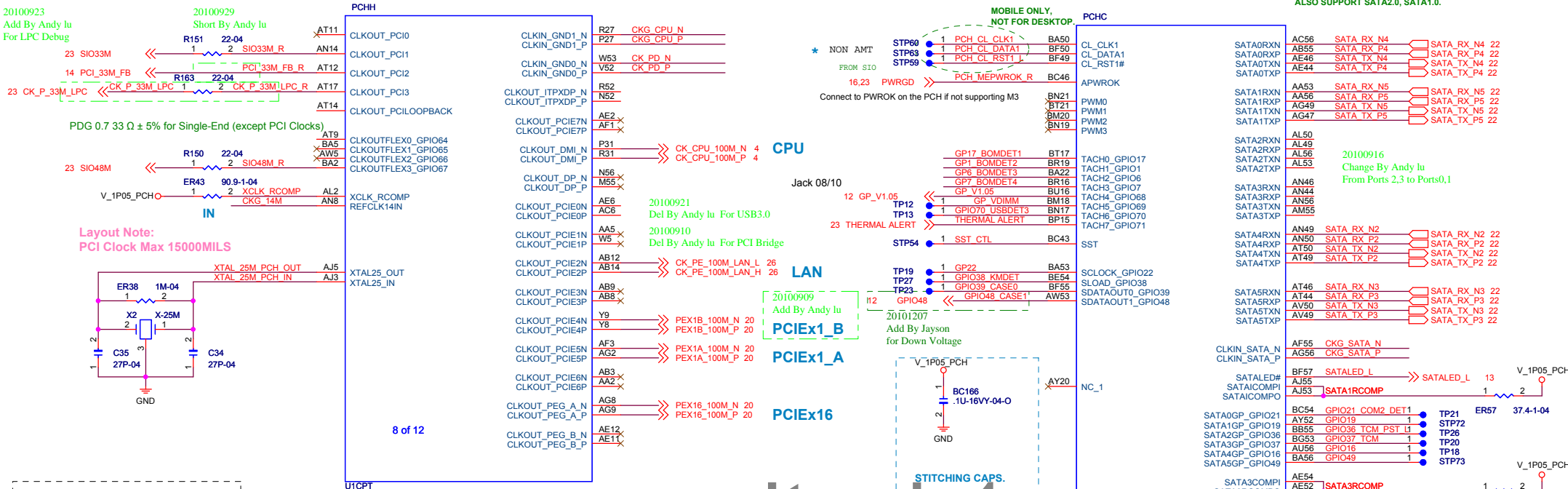
GNT[0..3]#
GPIO19
have been internal pull high to +VCC3

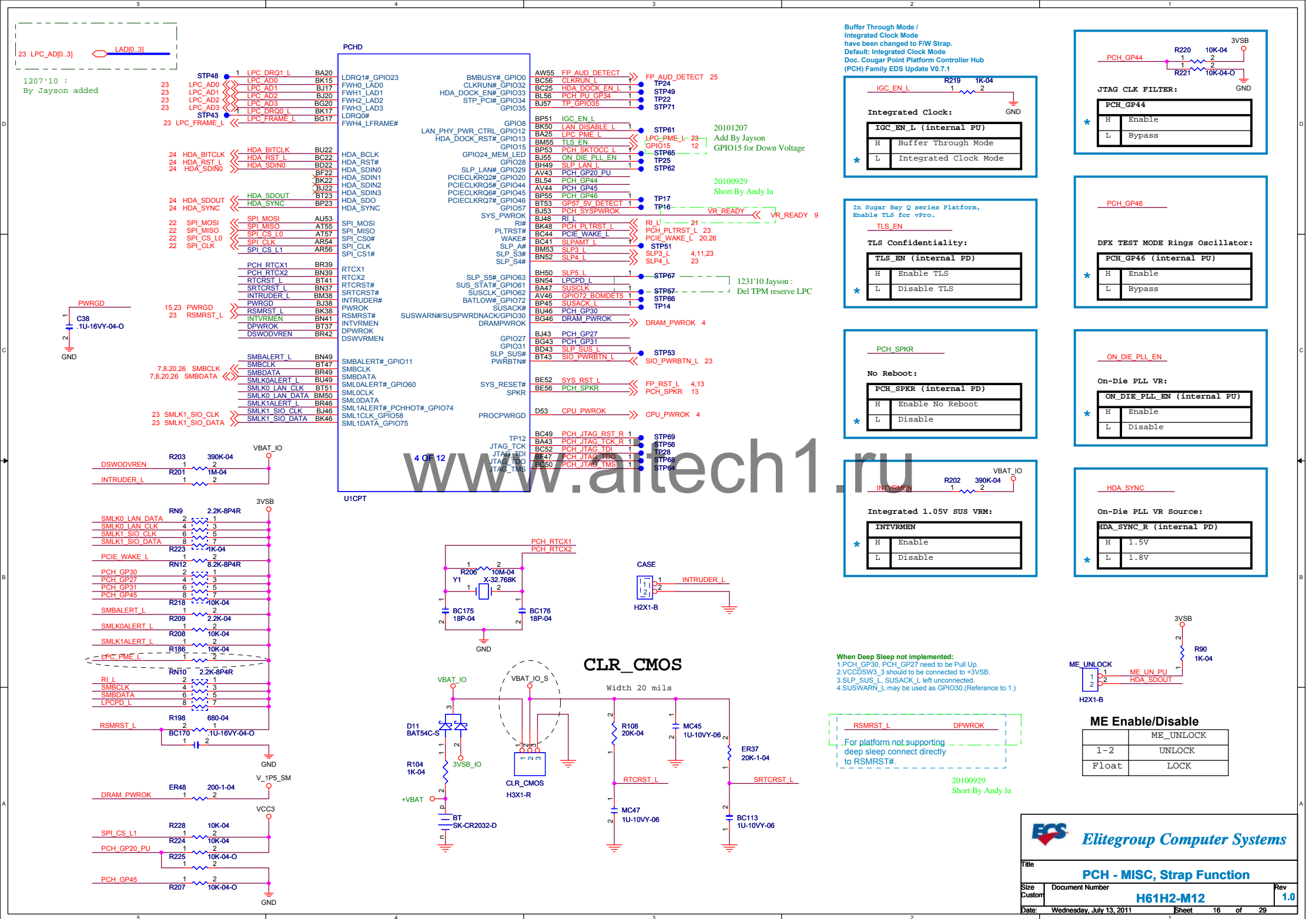
Boot Device Select:

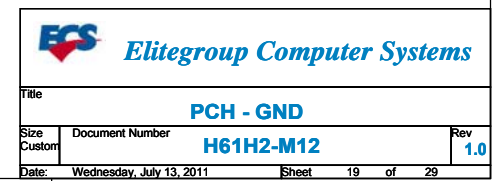
BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

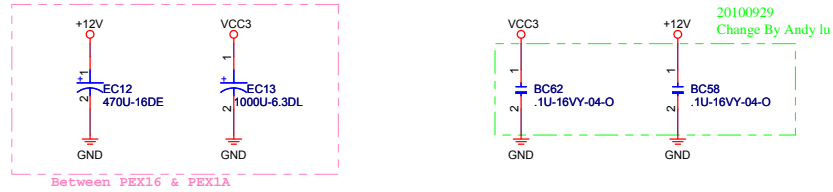
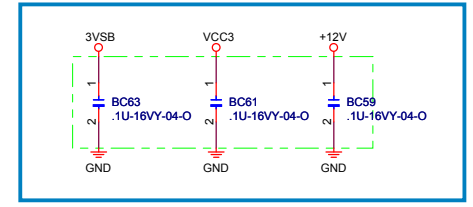
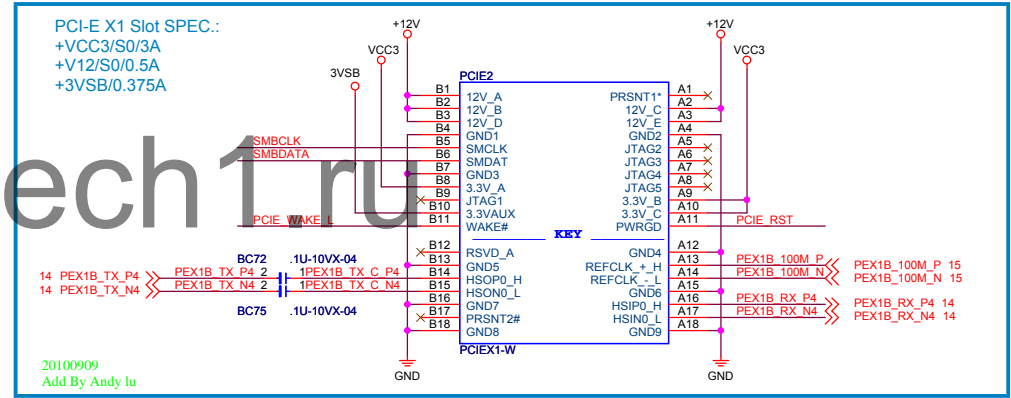
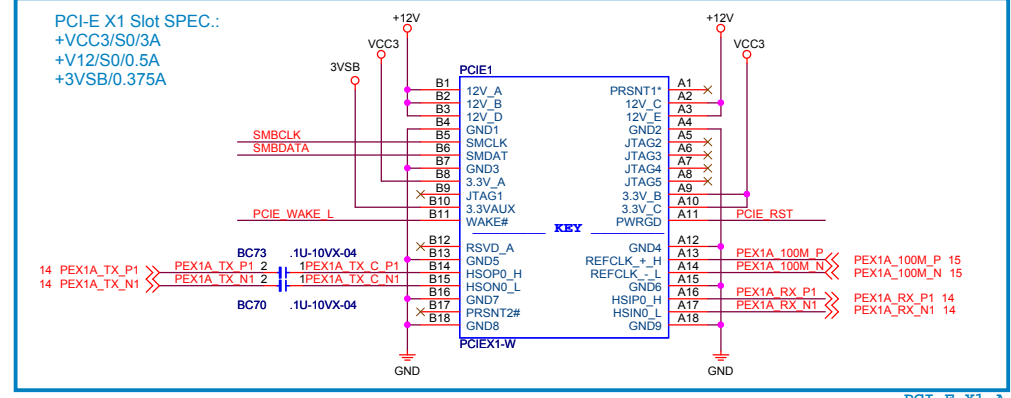
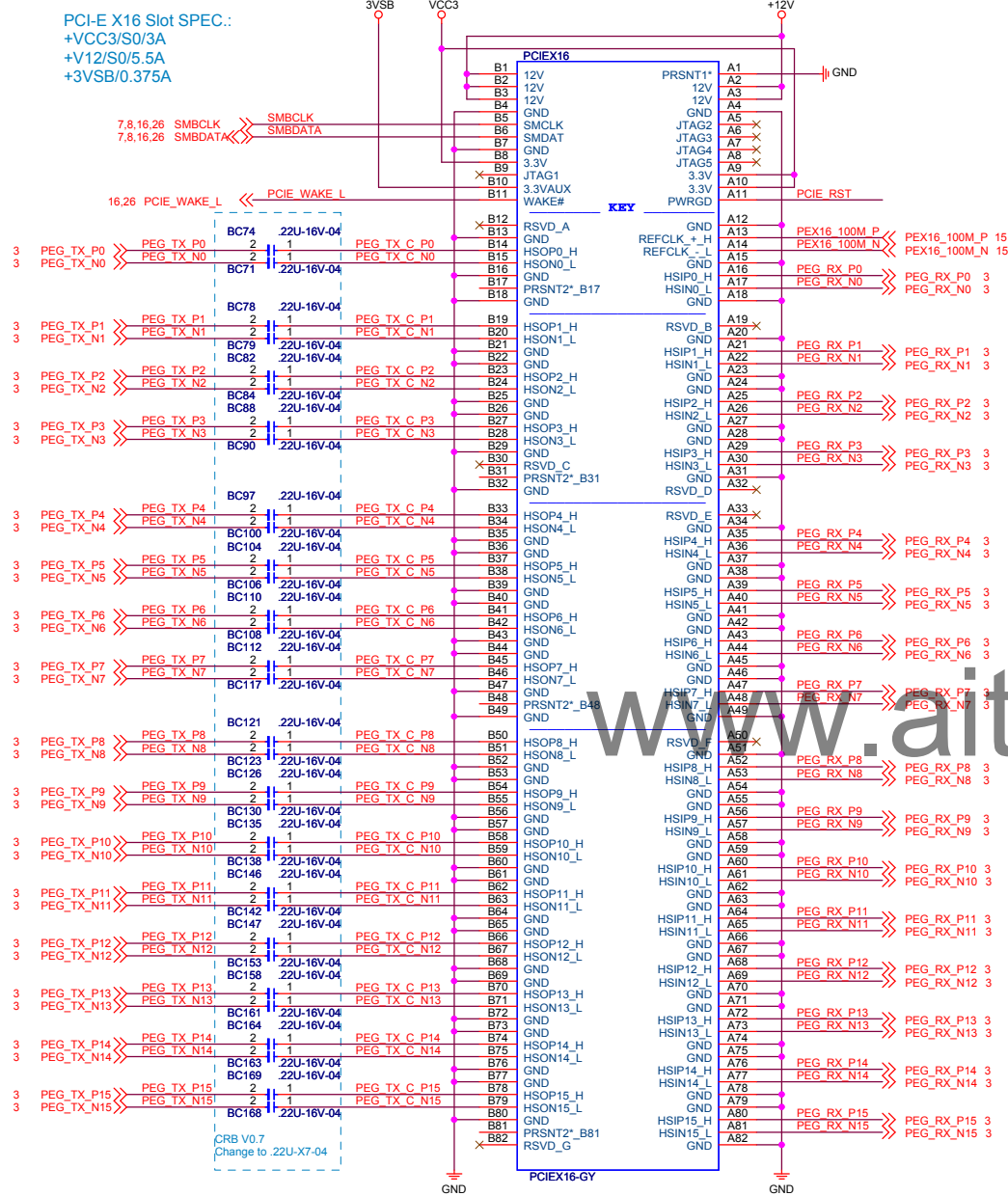


For H61:SATA port2/3 is disable....From 440377 file
**ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,
 ALSO SUPPORT SATA2.0, SATA1.0.**










```
0504'11 Jayson :  
DEL DVI
```

```
0504'11 Jayson :  
DEL DVI
```

```
0504'11 Jayson :  
DEL DVI Connector
```

```
0504'11 Jayson :  
DEL DVI
```

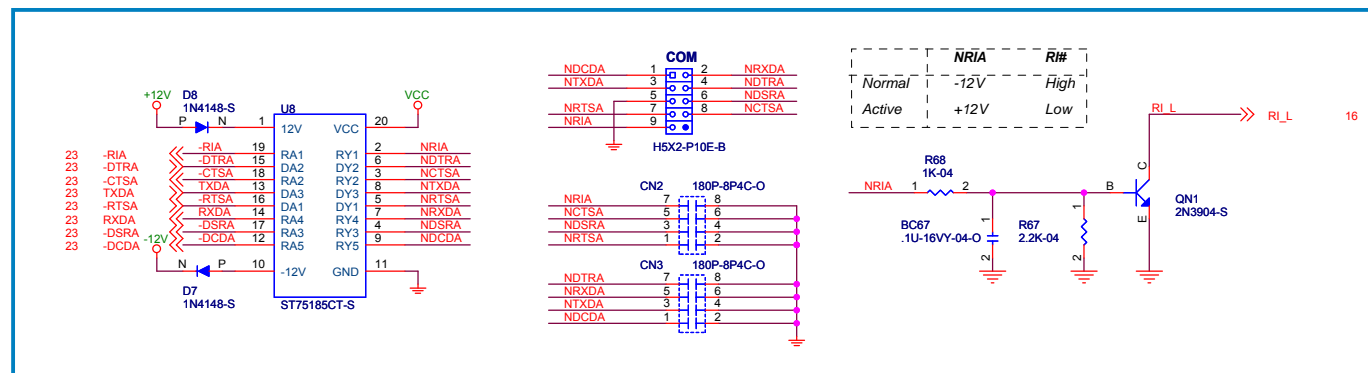
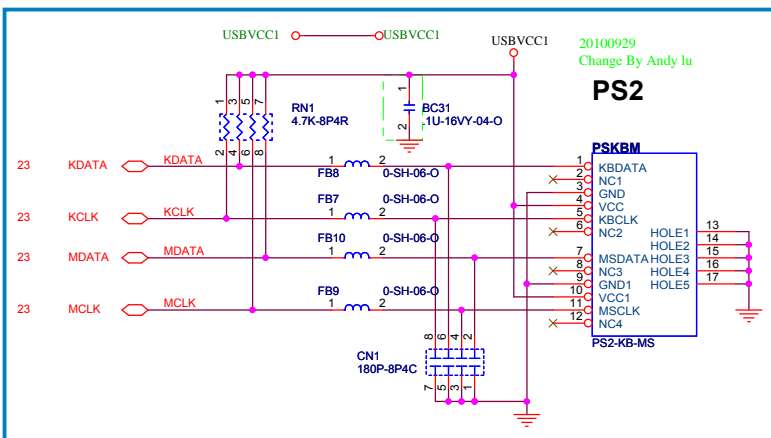
0504'11 Jayson :
DEL Fuse & Diode

```
0504'11 Jayson :  
DEL DVI
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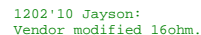
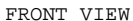
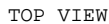
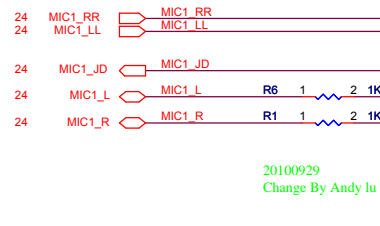
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```
1202'10 Jayson :  
Del HDMI
```

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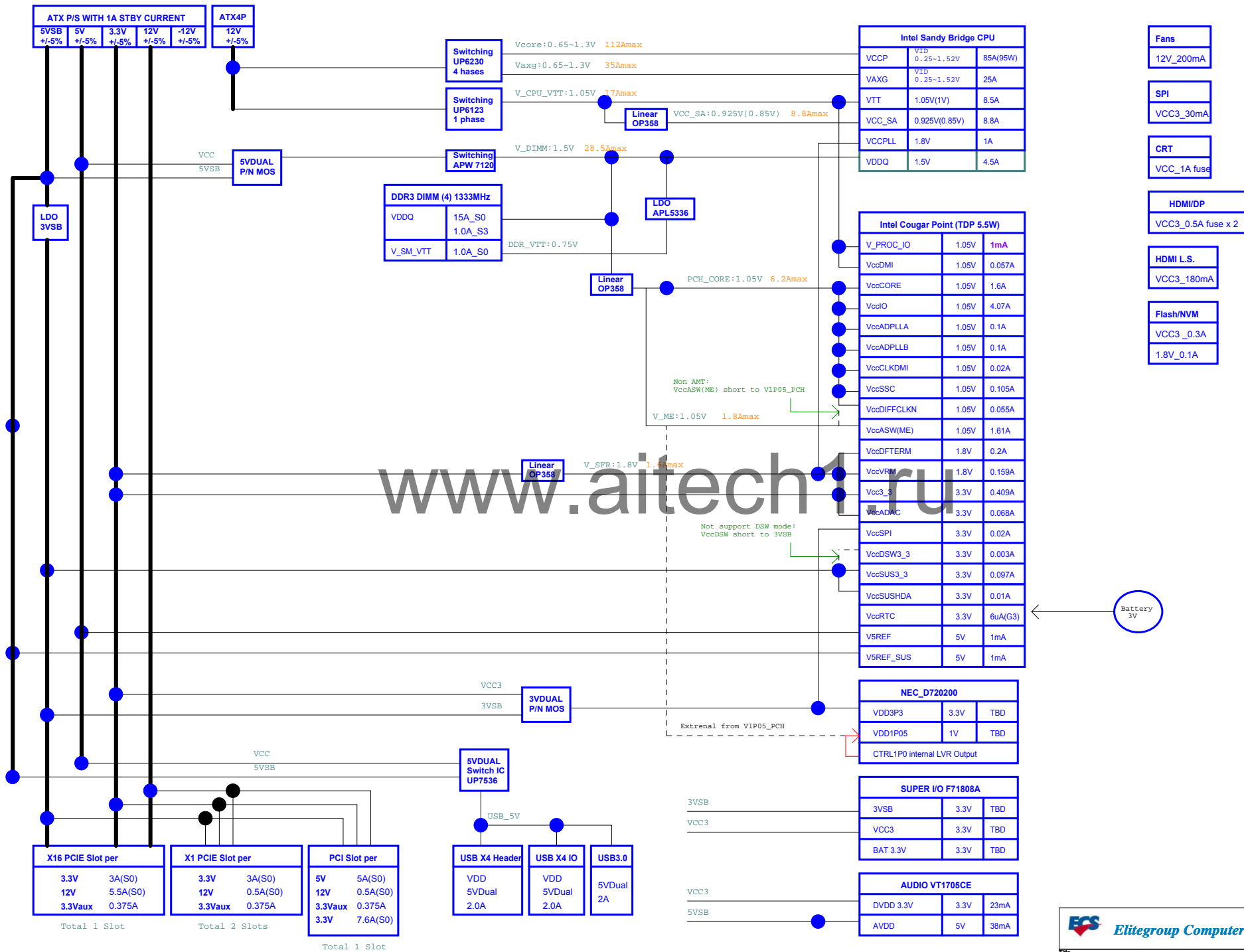


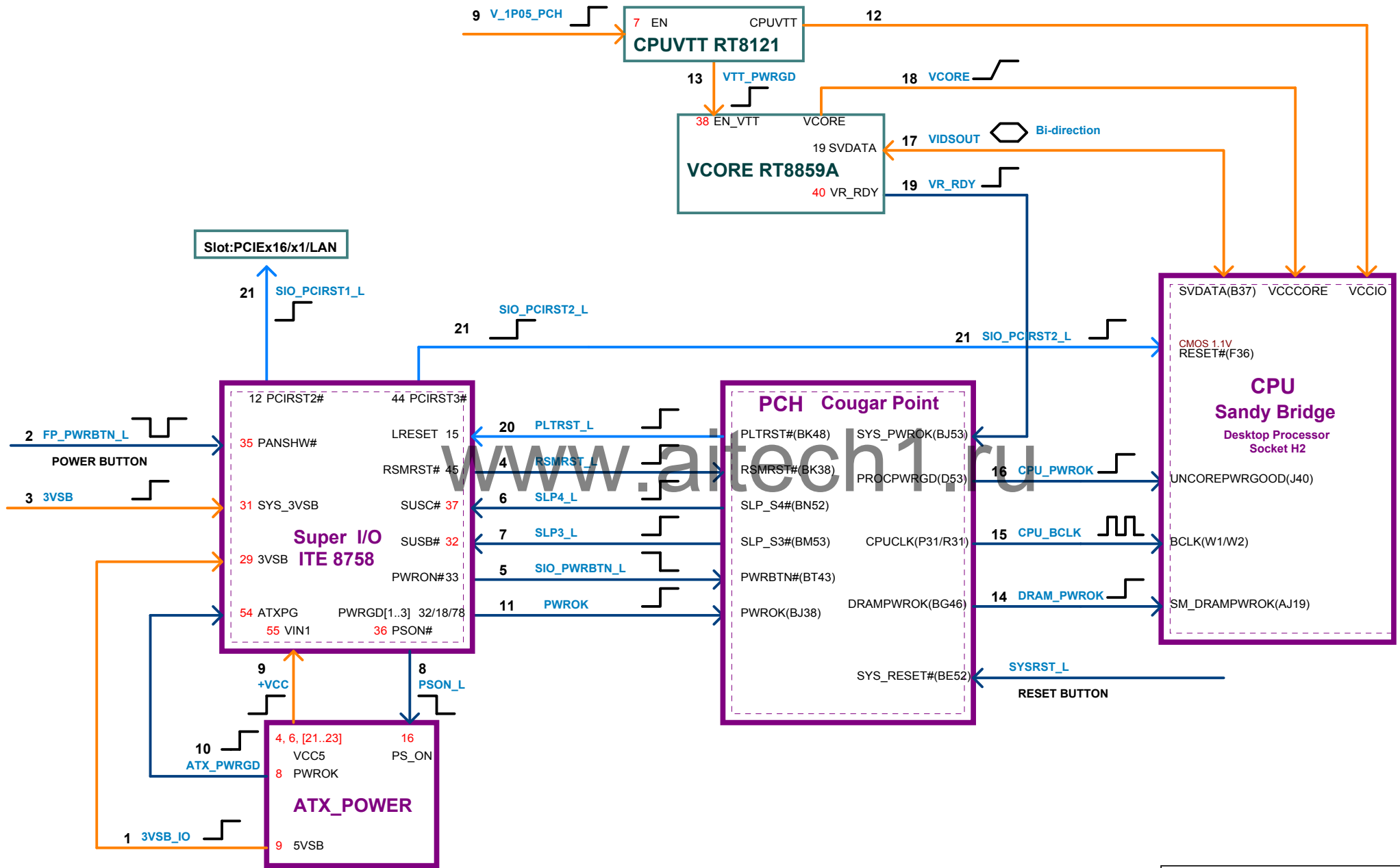
16 FP_AUD_DETECT << HDPANEL_DETECT



20100929
Change By Andy lu

1203'10 Jayson: Del SPDIF-OUT





NOTE:

Sugar Bay Platform has two clock mode:
1.Integrated Clock Mode (Generate by PCH)
2.Buffer Through Mode (Generate by Clock Gen.)
If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.
Please refer to
Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD
Page.13 PCH - SATA, SATA CONN for CLK IN PD
Page.14 PCH - MISC, F/W Strap
Page.15 PCH - CLK IO, CKG - CV184 for Option

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1129'10 By Jayson Del CK505

